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JC916 U.S. PTO 09/664094 09/19/00

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September 19, 2000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Masayuki MIZUNO
SEMICONDUCTOR INTEGRATED CIRCUIT
Our Ref. Q60884

Dear Sir:

Attached hereto is the application identified above including 19 sheets of the specification, claims, 4 sheets of formal drawings, executed Assignment and PTO 1595 form, and executed Declaration and Power of Attorney. Also enclosed is the Information Disclosure Statement with form PTO-1449 and references.

The Government filing fee is calculated as follows:

Total claims	9	-	20	=		x	$18.00	=	$.00
Independent claims	4	-	3	=	1	x	$78.00	=	$78.00
Base Fee									$690.00
TOTAL FILING FEE									**$768.00**
Recordation of Assignment									$40.00
TOTAL FEE									**$808.00**

Checks for the statutory filing fee of $768.00 and Assignment recordation fee of $40.00 are attached. You are also directed and authorized to charge or credit any difference or overpayment to Deposit Account No. 19-4880. The Commissioner is hereby authorized to charge any fees under 37 C.F.R. §§ 1.16 and 1.17 and any petitions for extension of time under 37 C.F.R. § 1.136 which may be required during the entire pendency of the application to Deposit Account No. 19-4880. A duplicate copy of this transmittal letter is attached.

Priority is claimed from September 20, 1999 based on Japanese Application No. 11-266203. The priority document is enclosed herewith.

Respectfully submitted,
SUGHRUE, MION, ZINN,
MACPEAK & SEAS, PLLC
Attorneys for Applicant

By: [signature]
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SEMICONDUCTOR INTEGRATED CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor integrated circuit, provided with an improved characteristic impedance of the signal transmission line of a semiconductor integrated circuit, capable of reducing coupling with other transmission lines.

Background Art

Conventionally, when providing a signal transmission line with a microstrip structure constituted by a signal line and a ground plate in a semiconductor integrated circuit, two separate wiring layers for the signal line and for the ground plate are used as shown in Fig. 8.

In order to increase the characteristic impedance of this signal transmission line in a signal transmission line of a microstrip structure composed of the integrated signal lines and a ground plate, two methods have been adopted, one method is to make the signal line width narrower, and the other method is to increase the distance d between the signal line and the ground plate.

Furthermore, the other conventional technique is disclosed in Japanese

Unexamined Patent Application, No. Hei 5-343564, which determines the characteristic impedance of the transmission line by a mesh-like mesh ground plane, and the spaces corresponding to the pores of the mesh are compensated for by the ground plate.

However, when the above-described first method for making the signal line width narrower is adopted, the problem arises that the maximum input capacitance of a circuit connected to the end of the signal transmission line becomes small.

When the above-described second method of increasing the distance d between the signal line and the ground plane is adopted, the problem is encountered that the thickness or the number of wiring layers increases, because it is necessary to increase the thickness of the interlayer films of the wiring layers or to increase the number of wiring layers.

When the third method disclosed in Japanese Unexamined Patent Application, First Publication No. Hei 5-343564 is adopted, although it is possible to increase the impedance of the signal transmission line, the problem arises that, when assembling into an integrated circuit, since the signal lines cannot be formed under the ground plane, it is not possible to avoid generating coupling between a plurality of signal lines.

When coupling occurs, a deficiency arises that in the characteristic impedance of a certain signal line will experience a dynamic change, because the capacitance between one signal line and its counter line changes when the voltage level of the counter signal line changes.

In addition, the problem also arises in the case of using a mesh ground plane that it is difficult to evaluate the characteristic impedance, since the electro-magnetic field generated through small holes or spaces cannot be accurately understood.

SUMMARY OF THE INVENTION

This invention has been made to solve the above-described problems. It is, therefore, an objective of the present invention to provide a semiconductor device, capable of reducing the coupling between a plurality of signal lines by increasing the characteristic impedance of the signal transmission line of a microstrip structure, which can be realized in a semiconductor device.

According to the first aspect of the present invention, a semiconductor integrated circuit comprises a signal transmission line of a microstrip structure composed of a signal line and a ground plate, wherein at least one hole is formed in said signal line.

According to the second aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate, at least one hole is formed in said ground plate.

According to the third aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the second aspect, the size of said

at least one hole formed in said ground plate is determined such that the AC coupling between the signal line and another signal line disposed close to one signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

According to the fourth aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the second aspect, the number of said at least one hole formed in said ground plate is determined such that the AC coupling between one signal line and another signal line disposed close to one signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

According to the fifth aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate, at least one hole is formed in both of said signal line and said ground plate.

According to the sixth aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the fifth aspect, the size of said at least one hole formed in said ground plate among the signal line and the ground plate is determined such that the AC coupling between one signal line and another signal line disposed close to one signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

According to the seventh aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the fifth aspect, the number of said at least one hole formed in said ground plate among holes formed in both of the signal line and the ground plate is determined such that the AC coupling between one signal line and another signal line disposed close to one signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

According to the eighth aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the second aspect, said at least one hole in said ground plate is formed at a position where the other signal line is not disposed or said at least one hole in said ground plate is made small so as to reduce the AC coupling with one signal line when formed at a position where the other signal line is disposed.

According to the ninth aspect, in a semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to the first aspect, where, instead of at least one hole formed in said signal line or in said ground plate, a plurality of slit holes are formed by forming said signal line or said ground plate of a plurality of thin strips and by connecting these thin strips at those terminal ends.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing the structure of the signal transmission line according to the first embodiment of the present invention.

Fig. 2 is a diagram showing the structure of the signal transmission line according to the second embodiment of the present invention.

Fig. 3A and Fig. 3B are diagrams showing the relationship between signal lines and a ground plate provided with a single slit.

Fig. 4 is a diagram showing the relationship between signal lines and a ground plate provided with the slit divided into three slits.

Fig. 5 is a graph showing the relationship between the slit width and magnitude of the coupling.

Fig. 6 is a graph showing the slit width in the ground plate and the characteristic impedance.

Fig. 7 is a diagram showing the structure of a signal transmission line according to the third embodiment of the present invention.

Fig. 8 is a diagram showing the structure of a conventional signal transmission line.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, the present embodiments of the present invention will be described with reference to the drawings.

<First Embodiment>

Fig. 1 is a diagram showing the structure of the signal transmission line according to the first embodiment of the present invention.

As shown in Fig. 1, in the signal transmission line of the microstrip structure realized in a semiconductor device according to the present embodiment, at least one hole 13 (normally, a plurality of holes 13) is formed on a signal line of a microstrip structure composed of a signal line 11 and a ground plate 12.

In a signal transmission line of the microstrip structure, the characteristic impedance Z is expressed by the equation,

$$Z = (L/C)^{1/2}$$

where C represents the inter-wiring capacitance per unit length, and L represents the inductance of the wiring.

The provision of a hole (or a plurality of holes) in the signal line 11 lengthen the electric force line generated between the signal line 11 and the ground plate 12 and the distance between the signal line 11 and the ground plate 12 is apparently elongated equivalently, which results in a decrease of the inter-wiring capacitance C.

When the velocity of the electro-magnetic wave is represented by v, the velocity v is constant and is expressed by the following equation.

$$v = 1/ (LC)^{1/2}$$

Thus, when the capacitance C decreases, the wiring inductance L increases.

Consequently, the characteristic impedance can be increased by forming more than one hole in the signal line.

In addition, the increase of the characteristic impedance as shown above makes it possible to suppress the reduction of the maximum input capacitance of the circuit connected at the end of the signal transmission line, and the increase of the characteristic impedance does not require an increase in the number of wiring layers.

The size of the hole 13 in the signal line shown in Fig. 1 can be determined as follows. The size of the hole is determined so as to reduce the wiring resistance as much as possible. At the same time, the size of the hole is determined so as to sufficiently increase the characteristic impedance between the signal line 11 and the ground plate 12 as much as possible.

The number of holes 13 in the signal line 11 may be determined so as to fulfill the following conditions. The number can be decreased to reduce the wiring resistance as much as possible, and the number can be increased to increase the characteristic impedance as much as possible.

It is noted that, instead of forming one signal line as shown in Fig. 1, the signal line may be formed by a plurality of signal line strips spaced apart from each other by slits and the plurality of signal line strips are connected at a certain portion such as both termination ends for forming a plurality of slit-like holes.

<Second Embodiment>

Fig. 2 is a diagram showing the structure of the signal transmission line according to the second embodiment of the present invention.

As shown in Fig. 2, in the signal transmission line of the microstrip structure realized in a semiconductor device according to the second embodiment, at least one hole 24 (normally, a plurality of holes 24) is formed on the ground plate 22 of a microstrip structure composed of a signal line 21 and a ground plate 22.

In the signal transmission line of the microstrip structure, the characteristic impedance Z is expressed by the equation,

$$Z = (L/C)^{1/2}$$

where C represents the inter-wiring capacitance per unit length, and L represents the inductance of the wiring.

The provision of a hole (or a plurality of holes) in the ground plate 22 lengthen the electric force line generated between the signal line 11 and the ground plate 12 and the distance between the signal line 11 and the ground plate 12 is apparently elongated equivalently, which results in a decrease of the inter-wiring capacitance C.

When the velocity of an electro-magnetic wave is represented by v, the velocity v is constant and is expressed by the following equation.

$$v = 1/ (LC)^{1/2}$$

Thus, when the capacitance C decreases, the wiring inductance L increases.

Consequently, the characteristic impedance can be increased by forming more than one hole in the ground plate 22.

As described above, it becomes possible to suppress the reduction of the maximum input capacitance of the circuit connected at the end of the signal transmission line, and it is not necessary to increase the number of wiring layers.

The size of the hole 24 in the ground plate shown in Fig. 2 can be determined as follows. The size of the hole is determined to reduce the AC coupling between two signal lines 21 adjacent to each other above the hole 24 in the ground plate 22 as much as possible. At the same time, the size of the hole is determined to sufficiently increase the characteristic impedance between the signal line 11 and the ground plate 12 as much as possible.

The number of holes 24 in the ground plate shown in Fig. 2 can be determined so as to fulfill the following conditions. The number can be decreased to reduce the AC coupling between two signal lines 21 adjacent to each other above hole 24 in the ground plate 22 as much as possible, and the number of the holes is determined to increase the characteristic impedance between the signal line 21 and the ground plate 22 as much as possible.

Next, the magnitude of the coupling and the characteristic impedance are explained based on the results of simulations in the case of forming the ground plate 22 by a plurality of ground plates, separated by slit-like spaces, with reference to Figs. 3 to 6.

Fig. 3A is a cross-sectional view of one transmission line comprising one signal line 21 of 1.2 μ m in width and 0.6 μ m in thickness, and a ground plate, divided into two plates, each having a width of 50 μ m, by a single slit of width w, wherein the ground plate is located spaced by a distance d from the signal line. Fig. 3B is a cross-sectional view of a transmission line comprising the signal line shown in Fig. 3A and a ground plate divided into four parts, having a width of 25 μ m, by three slits, each having a width of w/3, and these four parts are separated by three slits each having a width of w, wherein the ground plate is separated from the signal line by a distance of 0.6 μ m.

Fig. 4 is a schematic diagram showing the capacitance between one signal line 21 and a ground plate 22 having a slit, and the other signal line 23. It is assumed that the capacitance between the signal line 21 and the ground plate 22 is represented by Cg, and the capacitance between the signal line 21 and the other signal line 23 is represented by C_{13}.

Fig. 5 is a diagram showing the relationship between the total slit width and a value of C_{13}/Cg, wherein three lines are shown, in which the dashed line shows the case that the ground plate is divided by a single slit and the distance between the ground plate and the signal line is 0.6 μ m, the dashed and dotted line shows the case that the ground line is divided by a single slit and the distance between the ground plate and the signal line is 1.8 μ m, and the solid line shows the case that the ground plate is divided into four parts and the distance between the ground plate and the signal line is 0.6 μ m. It

is noted that the value of C_{13}/Cg represents the magnitude of the coupling between one signal line 21 with the other signal line 23.

In Fig. 5, when an allowable value of the coupling is assumed to be $C_{13}/Cg = 0.2$, the total slit widths in the respective cases must be restricted to within 3 μ m, 4.5 μ m, and 9 μ m or less, and the total slit width cannot exceed these values.

<Third Embodiment>

Fig. 7 is a diagram showing the structure of a semiconductor integrated circuit according to the third embodiment of the present invention.

As shown in Fig. 7, in the signal transmission line of the microstrip structure realized in a semiconductor device according to the present embodiment, at least one hole 33 (normally, a plurality of holes 33) is formed on the signal line and the ground plate of the microstrip structure composed of the signal line 31 and the ground plate 32.

In a signal transmission line of the microstrip structure, the characteristic impedance Z is expressed by the equation,

$$Z = (L/C)^{1/2}$$

where, C represents the inter-wiring capacitance at an unit length, and L represents the inductance of the wiring.

The provision of a hole (or a plurality of holes) in both of the signal line 31 and the ground plate 32 lengthen the electric force line generated between the signal line 31 and the ground plate 32 and the distance between the

signal line 31 and the ground plate 32 is apparently elongated equivalently, which results in a decrease of the inter-wiring capacitance C.

When the velocity of an electro-magnetic wave is represented by v, the velocity v is a constant and is expressed by the following equation.

$$v = 1/ (LC)^{1/2}$$

Thus, when the capacitance C decreases, the wiring inductance L increases.

Consequently, it becomes possible to suppress the reduction of the maximum input capacitance of the circuit connected at the end of the signal transmission line, and it is not necessary to increase the number of wiring layers.

The size of the hole 33 in the ground plate 32 shown in Fig. 7 can be determined as follows. The size of the hole is determined to reduce the AC coupling between two adjacent signal lines 31 on the hole 33 in the ground plate 32 as much as possible, and the size of the hole is determined to increase the characteristic impedance between the signal line 21 and the ground plate 32 as much as possible.

The number of holes is determined so as to reduce the AC coupling between two signal lines 31 adjacent on the hole 33 in the ground plate 32 as much as possible, and so as to increase the characteristic impedance between the signal line 31 and the ground plate 32 as much as possible.

It is noted that it may be possible, instead of forming holes in the signal line and the ground plate, to constitute the signal transmission line by

forming the signal line and the ground plate by a plurality of strips, and by connecting these strips at, for example, both termination ends of these strips so as to provide a plurality of slit-like holes between each of these strips.

The present invention was described above in detail by explaining the first to the third embodiments. However, the present invention is not limited to these three embodiments described above, but variants thereof can be envisaged without exceeding the scope of the present invention.

For example, the present invention includes the case of both of the signal line and the ground plate having holes together with slits.

Furthermore, in the above embodiments, one signal line is disposed on the ground plates. However, the ground plate may be disposed on the signal line, and the ground plate may occupy the most significant position. Such a disposition allows the ground plate to exhibit a shielding effect. In this case, the ground plate may be formed simultaneously with the formation of the bonding pads on the passivation film, which simplifies the manufacturing process.

As described above, in a signal transmission line of a microstrip structure composed of the signal line and the ground plate, the present invention shows a notable effect in that the capacitance between wiring can be decreased and the characteristic impedance between the signal line and the ground plate can be increased by forming holes in the signal line or in the ground plate.

The other effect of the present invention is that the coupling between

one signal line with another signal line through the ground plate can be reduced by forming holes in the ground plate.

What is claimed is:

1. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate, wherein at least one hole is formed in said signal line.

2. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate, wherein at least one hole is formed in said ground plate.

3. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 2, wherein the size of said at least one hole formed in said ground plate is determined such that the AC coupling between the signal line and another signal line disposed close to the signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

4. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 2, wherein the number of said at least one hole formed in said ground plate is determined such that the AC coupling between the

signal line and another signal line disposed close to the signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

5. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate, wherein at least one hole is formed in both of said signal line and said ground plate.

6. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 5, wherein the size of said at least one hole formed in said ground plate among the signal line and the ground plate is determined such that the AC coupling between the signal line and another signal line disposed close to the signal line and on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

7. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 5, wherein the number of said at least one hole formed in said ground plate among holes formed in both of the signal line and the ground plate is determined such that the AC coupling between the signal line

and another signal line disposed close to the signal line on the opposite side of said ground plate is decreased and the characteristic impedance of said signal transmission line is increased.

8. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 2, wherein said at least one hole in said ground plate is formed at a position where the other signal line is not disposed or said at least one hole in said ground plate is made small so as to reduce the AC coupling with one signal line when formed at a position where the other signal line is disposed.

9. A semiconductor integrated circuit comprising a signal transmission line of a microstrip structure composed of a signal line and a ground plate according to claim 1, wherein, instead of at least one hole formed in said signal line or in said ground plate, a plurality of slit holes are formed by forming said signal line or said ground plate of a plurality of thin strips and by connecting these thin strips at those terminal ends.

ABSTRACT

A semiconductor device comprising a signal transmission line of a microstrip structure, capable of increasing the characteristic impedance of the signal transmission line and reducing coupling between a plurality of signal lines. In a signal transmission line of a microstrip structure composed of a signal line and a ground plate, the capacitance between wires is reduced and the characteristic impedance can be increased by forming holes in the signal line or in the ground plate. The coupling between a plurality of signal lines can also be reduced.

FIG. 1

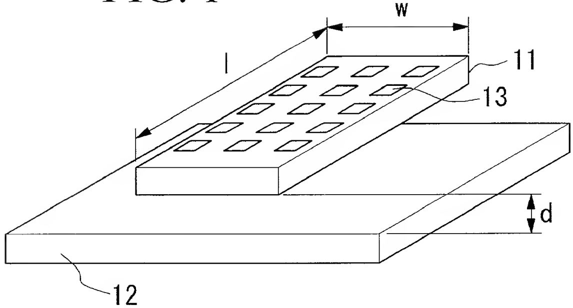


FIG. 2

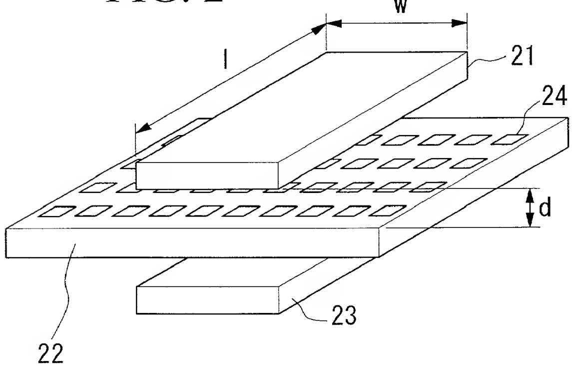


FIG. 3A

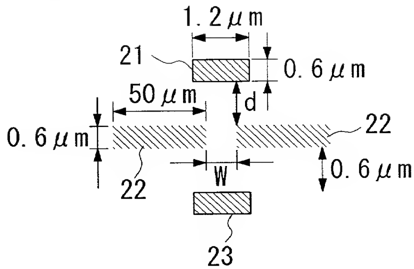


FIG. 3B

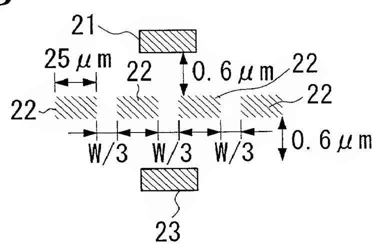


FIG. 4

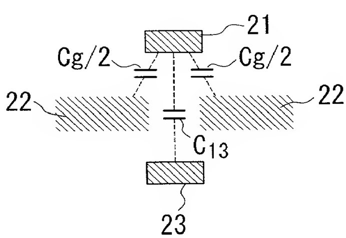


FIG. 5

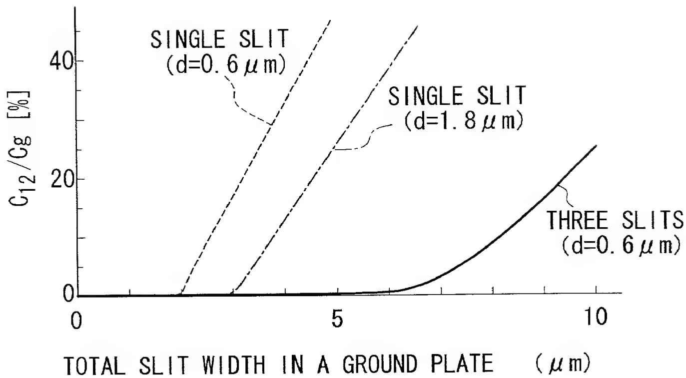

SINGLE SLIT
(d=0. 6 μm)
SINGLE SLIT
(d=1. 8 μm)
THREE SLITS
(d=0. 6 μm)
C12/Cg [%]
40
20
0
0
5
10
TOTAL SLIT WIDTH IN A GROUND PLATE (μm)

FIG. 6

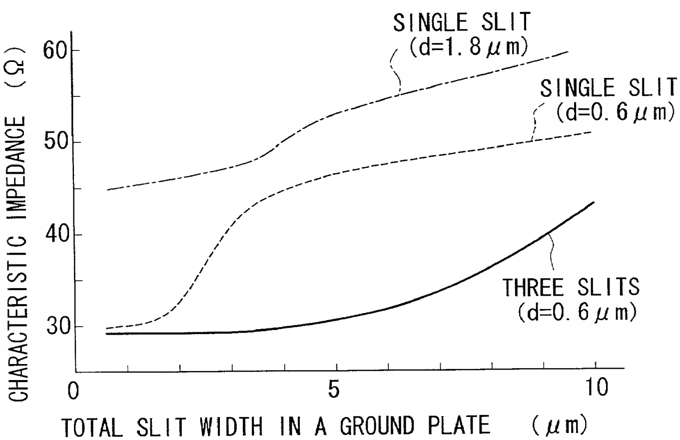

SINGLE SLIT
(d=1. 8 μm)
SINGLE SLIT
(d=0. 6 μm)
THREE SLITS
(d=0. 6 μm)
CHARACTERISTIC IMPEDANCE (Ω)
60
50
40
30
0
5
10
TOTAL SLIT WIDTH IN A GROUND PLATE (μm)

FIG. 7

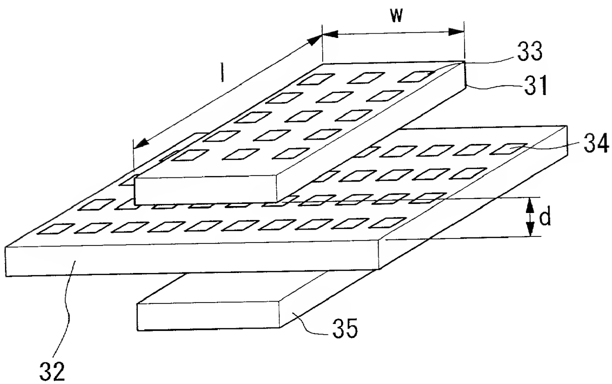
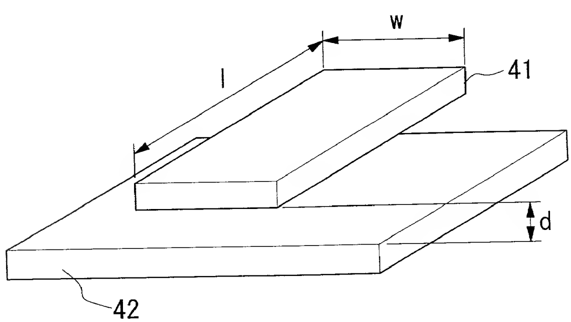


FIG. 8



99-266203 OSP-9582 US 𝟙/𝟙

SOLE/JOINT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name: that I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought in the application entitled:

SEMICONDUCTOR INTEGRATED CIRCUIT

which application is:

X the attached application (for original application)

___ application Serial No. _______________. filed _______________, and amended on _______________ (for declaration not accompanying application)

that I have reviewed and understand the contents of the specification of the above-identified application, including the claims, as amended by any amendment referred to above; that I acknowledge my duty to disclose information of which I am aware which is material to the patentability of this application under 37 C.F.R. 1.56, that I hereby claim foreign priority benefits under Title 35, United States Code §119, §172 or §365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified on said list any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

Application Number	Country	Filing Date	Priority Claimed (yes or no)
Patent 11-266203	Japan	20/09/1999	Yes

I hereby claim the benefit of Title 35, United States Code §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in a listed prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge my duty to disclose any information material to the patentability of this application under 37 C.F.R. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)

I hereby appoint John H. Mion, Reg. No. 18,879; Donald E. Zinn, Reg. No. 19,046; Thomas J. Macpeak, Reg. No. 19,292; Robert J. Seas, Jr., Reg. No. 21,092; Darryl Mexic, Reg. No. 23,063; Robert V. Sloan, Reg. No. 22,775; Peter D. Olexy, Reg. No. 24,513; J. Frank Osha, Reg. No. 24,625; Waddell A. Biggart, Reg. No. 24,861; Robert G. McMorrow, Reg. No. 19,093; Louis Gubinsky, Reg. No. 24,835; Neil B. Siegel, Reg. No. 25,200; David J. Cushing, Reg. No. 28,703; John R. Inge, Reg. No. 26,916; Joseph J. Ruch, Jr., Reg. No. 26,577; Sheldon I. Landsman, Reg. No. 25,430; Richard C. Turner, Reg. No. 29,710; Howard L. Bernstein, Reg. No. 25,665; Alan J. Kasper, Reg. No. 25,426; Kenneth J. Burchfiel, Reg. No. 31,333; Gordon Kit, Reg. No. 30,764; Susan J. Mack, Reg. No. 30,951; Frank L. Bernstein, Reg. No. 31,484; Mark Boland, Reg. No. 32,197; William H. Mandir, Reg. No. 32,156; Scott M. Daniels, Reg. No. 32,562; Brian W. Hannon, Reg. No. 32,778 and Abraham J. Rosner, Reg. No. 33,276, my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and request that all correspondence about the application be addressed to SUGHRUE, MION, ZINN, MACPEAK & SEAS, 2100 Pennsylvania Avenue, N.W., Washington, D.C. 20037-3202.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date September 12, 2000

First Inventor Masayuki Mizuno (First Name / Middle Initial / Last Name)

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Signature Masayuki Mizuno

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Citizenship Japan